Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) An internal voltage generating circuit in a semiconductor memory device, comprising:

a comparing means for comparing a voltage level of an internal voltage with that of a reference voltage;

a pull-up driving means for performing a pull-up operation for an output terminal in response to an output signal of the comparing means; and

a discharging means having two discharging units for discharging the output terminal in a period of which the voltage level of the internal voltage is higher than a predetermined target voltage level, wherein one of the two discharging units includes a plurality of active loads connected between the output terminal and a ground voltage in series.

2. (Previously Presented) The internal voltage generating circuit as recited in claim 1, wherein the discharge means includes:

a first discharge unit for discharging the output terminal when the voltage level of the internal voltage is higher than the predetermined target voltage level in response to the internal voltage; and

a second discharge unit for discharging the output terminal in response to a power supply voltage.

3. (Currently Amended) An internal voltage generating circuit in a semiconductor memory device, comprising:

a comparing means for comparing a voltage level of an internal voltage with that of a reference voltage;

a pull-up driving means for performing a pull-up operation for an output terminal in response to an output signal of the comparing means; and

a first discharging means for discharging the output terminal when the voltage level of the internal voltage is higher than a predetermined target voltage level in response to the internal voltage, wherein the first discharging means includes a plurality of active loads connected between the output terminal and a ground voltage in series[[.]] ; and

a second discharging means for discharging the output terminal in response to a power supply voltage.

4. (Canceled)

5. (Canceled)

6. (Previously Presented) The internal voltage generating circuit as recited in claim 3, wherein the first discharging means includes a plurality of diode-coupled NMOS transistors connected between the output terminal and a ground voltage in series

7. (Original) The internal voltage generating circuit as recited in claim 4, wherein the second discharge unit includes:

a voltage divider for producing a discharge control signal by dividing the power supply voltage; and

a discharge driver for performing a discharge operation of the output terminal in response to the discharge control signal.

8. (Original) The internal voltage generating circuit as recited in claim 7, wherein the voltage divider includes first and second resistors connected between the power supply voltage and the ground voltage in series.

9. (Original) The internal voltage generating circuit as recited in claim 8, wherein the discharge driver includes an NMOS transistor which is connected between the output terminal and the ground voltage and whose gate receives the discharge control signal.

10. (Original) The internal voltage generating circuit as recited in claim 3, wherein the pull-up driving means includes a PMOS transistor which is connected between the

power supply voltage and the output terminal and whose gate receives the output signal of the comparing means.

11. (Currently Amended) An internal voltage generating circuit in a semiconductor memory device, comprising:

a comparing unit to compare a voltage level of an internal voltage with that of a reference voltage;

a pull-up driving unit to perform a pull-up operation for an output terminal in response to an output signal of the comparing unit; and

a discharging unit configured to discharge the output terminal in a period of which the voltage level of the internal voltage is higher than a predetermined target voltage level, the discharging unit including first and second discharging components,

wherein one of the first discharging unit, the second discharging unit, and combination thereof ~~component~~ includes a plurality of active loads provided in series between the output terminal and the ground.

12. (Previously Presented) The internal voltage generating circuit of claim 11, wherein the first discharging component includes a plurality of diode-coupled NMOS transistors provided in series between the output terminal and the ground.

13. (Previously Presented) The internal voltage generating circuit of claim 11, wherein the second discharging component is configured to discharge the output terminal in response to the power supply voltage, and the first discharging component is configured to discharge the output terminal in response to the internal voltage.

14. (Previously Presented) The internal voltage generating circuit of claim 13, wherein the second discharge component includes:

a voltage divider to produce a discharge control signal by dividing the power supply voltage; and

a discharge driver to perform a discharge operation of the output terminal in response to the discharge control signal.

15. (Previously Presented) The internal voltage generating circuit of claim 14, wherein the voltage divider includes first and second resistors provided in series between the power supply voltage and the ground.

16. (Previously Presented) The internal voltage generating circuit of claim 15, wherein the discharge driver includes an NMOS transistor provided between the output terminal and the ground, the NMOS transistor having a gate that is configured to receive the discharge control signal.

17. (Previously Presented) The internal voltage generating circuit of claim 11, wherein the pull-up driving unit includes a PMOS transistor provided between the power supply voltage and the output terminal, the PMOS transistor having a gate that is configured to receive the output signal of the comparing unit.